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(54) **Delta-sigma modulator with switched capacitor implementation.**

(57) A Delta-Sigma modulator for one-bit analog to digital conversion of a signal (U(t)), such as a telephone voice channel signal to digital form is disclosed. The voice signal is sampled (1, 3, C_1) at a rate high compared to the highest voice channel frequency component. Sampled instantaneous signal values are integrated (4, C_3), re-sampled (10, 12, C_4) and again integrated (17, C_6) to reduce encoding noise. Finally, a bi-level sense identifying circuit (19) links the second integrator output to a D type flip-flop (20) providing the one-bit encoder output (b(n)).

The sampling and integrator control is effected by switching in a capacitor charge shifting arrangement under clock control and feedback is applied as a capacitor switching program modification (301, 302).

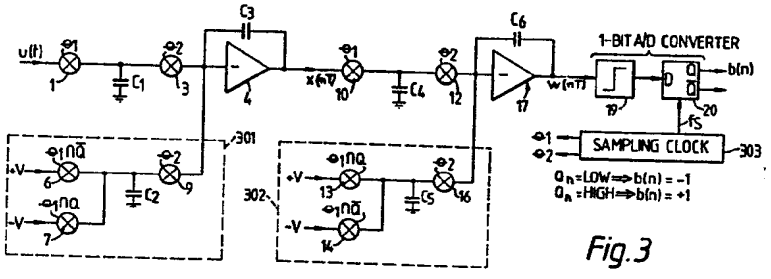

Fig.3

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Delta-Sigma Modulator with Switched Capacitor Implementation

The invention relates to a Delta-Sigma modulator for digitally encoding an analog input signal.

A modulator of this kind is disclosed in "IRE Transactions Space Electronics Telemetry", Vol. SET-8, pp. 204 - 209 (September 1962). In this paper the prior art, basically analog, delta-sigma modulator is presented and its utility as an improvement over the prior art Delta modulator is described.

The authors of the paper have pointed out that in the still earlier, so-called Delta modulation system, pulses are sent over a transmission line carrying information corresponding to the derivative of the input signal amplitude. At the receiving end, those pulses are integrated to obtain the original waveform. Transmission disturbances such as noise, etc., result in a cumulative error as a transmitted signal is integrated at the receiving end.

The so-called Delta-sigma modulation system provides for integration of the input signal before it enters the modulator itself so that the output transmitted pulses carry information corresponding to the amplitude of the input signal.

In a basically analog implementation, the behavior of a Delta-Sigma modulator depends on the absolute value of capacitors and resistors in the circuits and, therefore, sensivity to the detrimental effects of aging and temperature is encountered. Further, operational amplifiers included in analog implementations must be of superior quality, the gain and bandwidth of such amplifiers should not be such as to affect the transfer function of the integrator within the input circuitry of the device. Still further, in an analog implementation the waveform at the output of the digital to analog converter has to be precise and not pattern sensitive, that is, a pulse for an isolated "1" must be substantially identical to pulses imbedded in a series of "1-s". The circuit intricacies of analog Delta-Sigma modulator implementations are often the result of that requirement.

In view of the disadvantages of the prior art basically analog Delta-Sigma modulator, it is the general objective of the present invention to provide a Delta-Sigma modulator in which performance does not depend on the absolute value of capacitors and resistors as is the case with the prior art analog implementations. This object is attained as set forth in claim 1. Advantageous aspects and preferred embodiments are apparent from the subclaims.

The Delta-Sigma modulating characteristics are affected only by the ratio of capacitors. These ratios are relatively unaffected by temperature variations and aging. Absolute values of capacitors can be chosen so that the design of operational amplifiers is more flexible. For example, the larger the value of a capacitor, the larger is the slew rate requirement on the operational amplifier which is charging the capacitor. However, the stray capacitance will be more effectively swamped. Conversely, a small capaci-

tance is more easily charged, but the effect of stray capacitance is more pronounced. By leaving the absolute value of the capacitor as a design parameter, greater design latitude is possible in the overall Delta-Sigma modulator design.

Further, according to the switched capacitor implementation of the invention, operational amplifiers employed need only be able to charge and discharge circuit capacitors in a nominal time (on the order of one-half the sampling interval). The results in insensitivity to drift of element values caused by temperature and aging.

Further, a switched capacitor has an inherent sample and hold function at its input. Actually, the signals at all nodes in the circuit change at discrete instants of time. Consequently, the input to the comparator of the circuit is stable when the comparator makes a decision.

Basic circuitry, parameter identification and operational considerations are set forth in the detailed description of a preferred embodiment of the invention hereinafter presented.

Fig. 1 is a schematic block diagram representative of typical analog implementations according to the prior art.

Fig. 2 is a schematic block diagram basically representative of switched capacitor implementations.

Fig. 3 is a schematic diagram of an implementation of the Delta-Sigma modulator according to the invention employing +V and -V reference voltages.

Fig. 4 is a timing waveform presentation for the circuit of Fig. 3.

Fig. 5 shows a portion of a circuit of Fig. 4 with circuitry adapated to the use of a single reference voltage +V.

Fig. 6 illustrates the substitution of the single reference voltage circuitry of Fig. 5 into the device of Fig.3.

At the outset, it should be pointed out that the term Delta-Sigma modulator is sometimes called a Sigma-Delta modulator, the transposition of the sigma and delta terms being a matter of author's preference, the same device going under either name. Fig. 1 is prior art as aforementioned and substantially self-explanatory. In Fig. 1 herewith, the D/A converter would be a pulse shaper providing one of the two different pulses in accordance with whether the digital signal is high or low, mathematicly +A or -A, the quantity A being related to the conversion between a number and a voltage. The basically lowpass (integrating) device labeled H(s) determines the order of the Delta-Sigma modulator. H(s) is typically a first order filter if H(s) is $= \frac{g}{s}$ and second order

$$\text{if } H(s) = \frac{g\ (s+C)}{(s+a)\ (s+b)}$$

It may be said that the modulator noise (inaccuracy of conversion of the input function to a digital signal) reduction achieved by the Delta-Sigma modulator is the result of keeping track of all previous conversion errors and feeding this information (as an error related signal) back to correct the next conversion. In this process, a first order modulator attempts to zero the average error over a period of time, whereas a second order modulator not only keeps

this average error at zero but also keeps the first derivative of the error signal at zero.

In a first order system, only a DC input signal will be accurately represented digitally. However, in a second order system, the bandwidth of the signal which can be continuously represented digitally is increased.

According to known filter theory, the integrating filter H(s) can be described for a first order Delta-Sigma modulator as:

$$H(s) = \frac{\alpha+\beta s}{1+\eta s}, \text{ and}$$

similarly, for a second order filter

$$H(s) = \frac{\alpha+\beta s+\delta s}{1+\eta s+s^2}$$

Capacitor and other component values are chosen to give appropriate values for the coefficients. Delta-Sigma modulation performance in terms of noise and stability is related to these coefficients. The paper cited hereinbefore provides an implementation and the underlying analysis of a "first-order" Delta-Sigma modulator. Figure 1 of that paper shows the "error signal", S(t) - P(t) being applied to an integrator which has a first-order transfer-function and consequently is a "first-order Delta-Sigma modulator".

In Fig. 1 of that paper, the sampling pulse generator and pulse modulator together form an A/D + D/A operation. The pulse modulator outputs a pulse of known shape whose polarity is determined by the polarity of the analog signal at the input of the pulse modulator at the instant the sampling pulse is asserted.

Higher order Delta-Sigma modulators provide, potentially, better noise behavior but are notorious for being unstable and are consequently not recommended. The second order embodiment herein described is regarded as optimum.

All switched capacitor implementations are generalized in Fig. 2 and can be, mathematically, reduced to the form shown below.

H(z) is a discrete-time transfer function, of the form (for "second-order Delta-Sigma Modulator"):

$$H(z) = z^{-1}\left[\frac{\alpha+\beta z^{-1}+\eta z^{-2}}{1+\delta z^{-1}+ z^{-2}}\right]\gamma$$

where z^{-1} is the unit delay operator, unit delay being the time of one sampling interval. For a sampling rate of 1 MHz, the sampling interval will be seen to be 1 μs. The coefficients, which determine the noise performance and stability, are functions of capacitor ratios. The absolute value of each capacitor can be chosen by the circuit designer to optimize amplifier performance, to swamp stray capacitance, etc.

The switched capacitor Delta-Sigma modulator according to the invention is best explained in stages. The principle underlying the operation of any Delta-Sigma modulator is to provide an analog-to-digital conversion wherein the digital word size is small but the sampling frequency is much higher than the highest signal (speech) frequency.

First consider the sampling clock which operates the D type (edge-triggered) flip-flop, 20 in Fig. 3. This clock provides the time reference f_s and also two other clock waveforms, at the sampling frequency, but with duty cycle less

than 50 %. These are designated θ_1 ("charge") and θ_2 ("discharge"). Fig. 4 depicts these waveforms in a typical relationship.

Consider next a section of Fig. 3 consisting of switches 1 and 3, capacitor C_1, amplifier 4 and capacitor C_3. Here θ_1 from sampling clock 303 controls the switch 1 and θ_2 controls the switch 3. When θ_1 is low, switch 1 is open (open circuit) and when θ_1 is high, switch 1 is closed (short circuit). Similarly with θ_2 and switch 3. The non-overlapping nature of θ_1 and θ_2 ensures that switches 1 and 3 will not both be closed at any time. Assuming the input signal u(t) remains constant over the inverval $[nT, (n+1)T]$, capacitor C_1 will charge during θ_1, to a voltage equal to u(nT). Assuming the amplifier, 4, is an ideal op-amp, during θ_2 all the charge on C_1 will be transferred to C_3, causing a change in the voltage across C_3 of $-\frac{C_1\ u(nT)}{C_3}$. Consequently, at t = (n+1)T, the op-amp output voltage, x, will be

$$x\left[(n+1)T\right] = x(nT) - \left(\frac{C_1}{C_3}\right) u(nT),$$

the negative increment is because the amplifier inverts. Now consider the addition of switches 6, 7 and 9 and capacitor C_2. If b(n) is +1, i.e. Qn = HIGH, then during θ_1, C_2 would charge to -V. In short C_2 would charge to $-b(n)\cdot V$. During θ_2 this charge would be transferred to C_3. The overall operation of switches 1, 3, 6, 7 and 9 and capacitors C_1, C_2 and C_3, and amplifier 4 can be described by the equation:

$$x\left[(n+1)T\right] = x(nT) - \left(\frac{C_1}{C_3}\right) u(nT) + b(n)\cdot V\cdot\left(\frac{C_1}{C_3}\right)$$

similarly,

$$w\left[(n+1)T\right] = w(nT) - \left(\frac{C_4}{C_6}\right) x(nT) - b(n) \cdot V \cdot \left(\frac{C_5}{C_6}\right)$$

The dotted enclosures 301 and 302 may be called reference switching means. The operation of the comparator and D flip-flop is to obtain

$$b(n+1) = \text{sgn}\left\{w\left[(n+1)T\right]\right\}.$$

The noise performance and stability of the Delta-Sigma modulator is governed by the capacitor ratios

$\left(\frac{C_1}{C_3}\right)$, $\left(\frac{C_2}{C_3}\right)$, $\left(\frac{C_4}{C_6}\right)$ and $\left(\frac{C_5}{C_6}\right)$.

The voltage V is termed the "reference voltage" and normally all voltages are evaluated as fractions thereof. V ist sometimes referred to as the "crash point" of the encoder and is the maximum amplitude of the input signal. An input amplitude of greater than V will cause overload.

For a typical Delta-Sigma modulator, the following capacitor ratios were found to be satisfactory.

$$\left(\frac{C_1}{C_3}\right) = \left(\frac{C_2}{C_3}\right) = \frac{1}{2}$$

$$\left(\frac{C_4}{C_6}\right) = \left(\frac{C_5}{C_6}\right) = 1$$

It will be noted that the configuration of Fig. 3 requires two reference voltages, +V and -V. If only one reference, for example +V is available, then the configuration consisting of +V, -V, switches 6, 7 and 9 and capacitor C_2 (similarly with +V, -V, switches 13, 14, 16 and capacitor

C_5) can be replaced by the circuit 501 shown in Fig. 5 and included in Fig. 6 as dotted block 601.

In that variation, and during each sampling interval, C_8 charges to V during θ_1 and during θ_2

causing a change of $-\left(\frac{C_8}{C_3}\right) \cdot V$ in the output of amplifier 4.

During θ_1, C_7 charges to V volts with the polarity indicated shown on Figs. 5 and 6. If Q_n were "high", i.e., b(n) = +1, switches 23 and 22 would close during θ_2 and, because of the polarity reversal, cause a change of $+\left(\frac{C_7}{C_3}\right) \cdot V$ in the output of amplifier 4. If b(n) = -1, then C_7 does not discharge into C_3. The net effect is then:

$$\text{if } b(n) = +1 \qquad \Delta x = \left(\frac{C_7}{C_3} - \frac{C_8}{C_3}\right) \cdot V - \left(\frac{C_1}{C_3}\right) \cdot u(nT)$$

$$\text{or if } b(n) = -1 \qquad \Delta x = -\left(\frac{C_8}{C_3}\right) \cdot V - \left(\frac{C_1}{C_3}\right) \cdot u(nT) .$$

If $C_7 = 2C_8$, then the overall operation of the circuit in Fig. 5 can be described as

$$x\left[(n+1)T\right] = x(nT) - \left(\frac{C_1}{C_3}\right) \cdot u(nT) + b(n)V \cdot \left(\frac{C_8}{C_3}\right)$$

similarly

$$w\left[(n+1)T\right] = w(nT) - \left(\frac{C_4}{C_6}\right) \cdot x(nT) - b(n)V \cdot \left(\frac{C_{10}}{C_6}\right) .$$

Implementing the Delta-Sigma modulator of the invention according to Fig. 6, the following capacitor ratios would be used:

$$\frac{C_8}{C_3} = \frac{C_1}{C_3} = \frac{1}{2}$$

$$\frac{C_4}{C_6} = \frac{C_{10}}{C_6} = 1$$

$$\frac{C_7}{C_8} = \frac{C_9}{C_{10}} = 2.$$

The samling rate must be much higher than the highest frequency component of the input signal u(t). The invention is particularly useful for digitally encoding telephone (speech) band signals for transmission through a discrete telephonic channel. Since such signals require only a few kHz of bandwidth, and accordingly the sampling rate of 1 MHz typical for the modulator of the invention fulfills the aforementioned requirement. A second order Delta-Sigma modulator can be considered to be constructed of a first order Delta-Sigma modulator embedded in a feedback loop. Conversely, a first order Delta-Sigma modulator can be considered to be a subset of a second order Delta-Sigma modulator obtained by "stripping" the second order Delta-Sigma modulator down. The configuration shown in Figures 3 or 6 be stripped down to form a first order switched capacitor Delta-Sigma modulator. If amplifier 4, capacitors C_3, C_1, C_2 and their associated switches are removed, what remains is a first order Delta-Sigma modulator which converts an analog signal at u into a digital signal b(n).

It is possible to transmit the bit-stream $\{b(n)\}$ as is and at the receiving end have a simple digital-to-analog converter which comprises of a pulse shaper which puts out distinct waveforms in a bit-inverval according as b(n) = "HIGH" or b(n) = "LOW" followed by a simple analog lowpass

filter to smooth the waveform. This, however, would entail the transmission of $\{b(n)\}$ directly, which is about 1 megabit/s which is quite high. An alternative method, is to employ a sequence of digital lowpass filters which do the "smooting" while retaining the digital nature of the signal. As a consequence, the number of bits per word increases, that is the granularity of levels, which can be represented, is made fine. In a line circuit such as that of U.S. Patent No. 4,270,027 the lowpass filters permit the resampling of the digital signal at 8 Kilowords per sec with a granularity corresponding to 13 bits per word in a uniform code. Each code word can be converted into an 8-bit code, if so desired, corresponding to either the A-law or μ-law format. The 1-bit device, in this sense, does represent a large range of sample values from u(nt). The 1-bit/word, 1 Mword/sec stream (i.e. a 1-Megabit/sec stream) is sometaimes referred to in the art as "PULSE-DENSITY MODULATED" version of the complex voice channel signal.

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Claims

1. A Delta-Sigma modulator for digitally encoding an analog input signal, characterized in that it comprises:

- clock means (303) for generating a timing waveform (f_S) having a frequency substantially higher than the highest frequency component of said analog input signal;

- a sampling circuit (1, 3, C_1) including switching capacitance means for storing charge representative of instantaneous amplitude values of said analog input signal (u(t));

- integrating means (4, C_3) operative as a lowpass filter responsive to the output of said sampling circuit (1, 3, C_1);

- a one-bit analog-to-digital converter (19, 20) clocked by said timing waveform (f_S) and providing first and second outputs (Q, $\overline{Q}$) in response to the instantaneous polarity of the output signal of said integrating means (4, C_3), said second output ($\overline{Q}$) being complementary of said first output (Q);

- reference means (301) for selectively applying a charging voltage to said integrating means (4, C_3).

2. A Delta-Sigma modulator as claimed in claim 1, characterized in that it further comprises:

- a second sampling circuit including switching capacitance means (10, 12, C_4) for storing charge representative of instantaneous amplitude values of the output signal (X(nT)) of said first integrating means (4, C_3);

- second integrating means (17, C_6) operative as a second lowpass filter responsive to the output of said second sampling circuit (10, 12, C_4), said one-bit analog-to-digital converter (19, 20) being responsive to the output signal of said second integrating means (17, C_6) and
- second reference means (302) for selectively applying a charging voltage to said second integrating means (17, C_6) (Fig. 3).

3. A Delta-Sigma modulator as claimed in claims 1 or 2, characterized in that

- said clock means (303) generate, in addition, to said timing waveform (f_s) having first and second levels, first and second switching gates (θ_1, θ_2) within the duration of, but not overlapping said timing gate waveform first and second levels;

- said first and second sampling circuits (1, 3, C_1, 10, 12, C_4) are each operated to store during said first switching gate (θ_1) charge representative of the instantaneous amplitude value of their respective analog input signal and to output said stored charge during

said second switching gate (θ_2), said first and second sampling circuits comprising first and second capacitors (C_1, C_4) for charge storage and switching means associated therewith;

- said first reference means (301) include a third capacitor (C_2) and additional switching means (6, 7, 9) connected to charge said third capacitor (C_2) to +V or -V reference voltage during said first switching gate (θ_1) in polarity corresponding to $\theta_1 n\bar{Q}$ or $\theta_1 nQ$, respectively, where θ_1 is said first switching gate and to apply said third capcitor voltage to said first integrating means input during said second switching gate (θ_2);

- and said second reference means (302) include a fourth capacitor (C_5) and second additional switching means (13, 14, 16) connected to charge said fourth capacitor (C_5) to +V or -V reference voltage during said first switching gate (θ_1) in polarity corresponding to $\theta_1 nQ$ or $\theta_1 n\ \bar{Q}$, respectively, and to apply said fourth capacitor voltage to said second integrating means input during said second switching gate (θ_2) (Fig. 3).

4. A Delta-Sigma modulator as claimed in any one of the preceding claims, characterized in that said first and second integrators comprise corresponding inverting first and second operational amplifiers (4, 17) having fifth and sixth capacitors (C_3, C_6), connected between input and output of said first and second amplifiers (4, 17), respectively (Fig. 3, Fig. 6).

5. A Delta-Sigmal modulator as claimed in any one of the preceding claims, characterized in that said one-bit analog-to-digital converter comprises a comparator (19) responding to

the preceding integrator to provide a polarity responsive output having a first or second condition, and a D type flip-flop circuit (20) responsive to said comparator output for providing Q and $\bar{Q}$ outputs, said Q output providing the one-bit code (Fig. 3, Fig. 6).

6. A Delta-Sigma modulator as claimed in claim 4, characterized in that the ratio of the capacitance of said first capacitor (C_1) to that of said fifth capacitor (C_3) and the capacitance ratio of said third capacitor (C_2) to that of said fifth capacitor (C_3) is approximately 1/2; the ratio of the capacitance of said second capacitor (C_4) to that of said sixth capacitor (C_6) and the capacitance ratio of said fourth capacitor (C_5) to that of said sixth capacitor (C_6) being unity (Fig. 3, Fig. 6).

7. A Delta-Sigma modulator as claimed in any one of the preceding claims, characterized in that said clock means (303) is further defined as generating said switching gates (θ_1, θ_2) each substantially time-centered with the duration of the corresponding timing gate waveform first and second levels (Fig. 4).

8. A Delta-Sigma modulator as claimed in any one of the preceding claims, characterized in that said first reference means (601) includes additional switching means (22, 24) associated with said third capacitor (7) for switching the terminal of said third capacitor (C_7) which is connected to ground potential to the positive terminal thereof during the time of $\theta_2 \cap Q$ and to the negative terminal thereof during θ_1, said third capacitor voltage being outputted to said first integrating means (4, C_3) during $\theta_2 \cap Q$, said second reference means (602) comprising second additional switching means (30, 33) associated with said fourth capacitor (C_9) for switching the terminal thereof which is connected to

ground potential to the positive terminal thereof during the time $\theta_2 n\bar{Q}$ and to the negative terminal during θ_1, said fourth capacitor voltage being outputted to said second integrating means (17, C_6) during $\theta_2 n\bar{Q}$, thereby to provide the function of said reference means using only a positive reference voltage (+V) (Fig. 5, Fig. 6).

9. A Delta-Sigma modulator as claimed in any one of the preceding claims, characterized in that said switching means comprise individual signal controlled electronic switches.

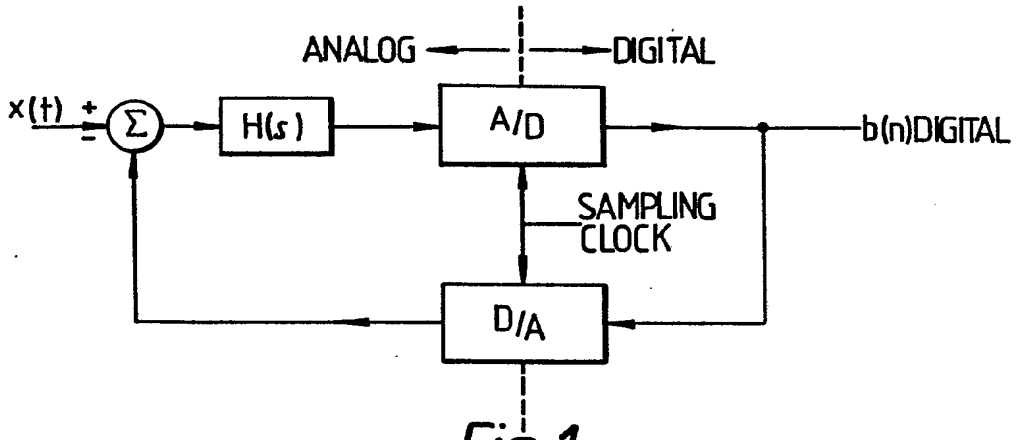


Fig.1 PRIOR ART

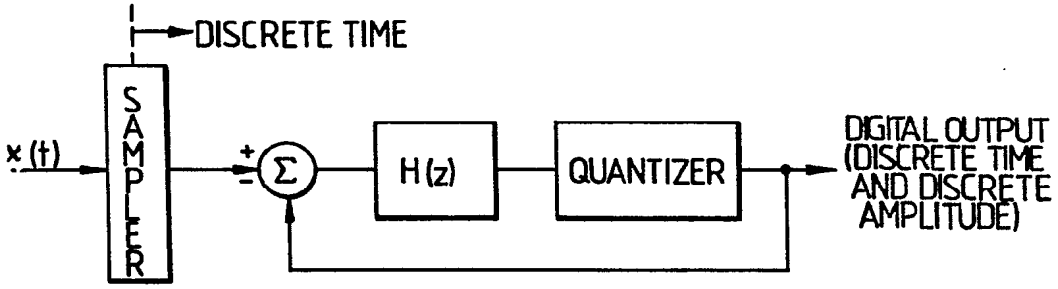


Fig. 2

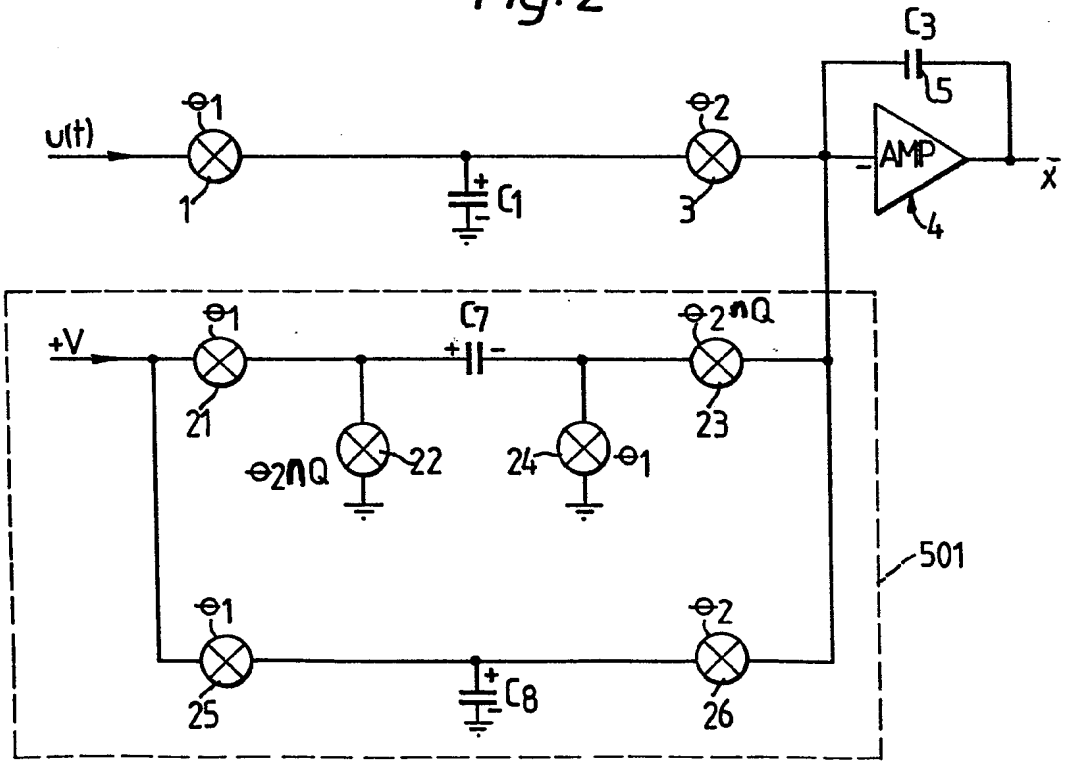


Fig. 5

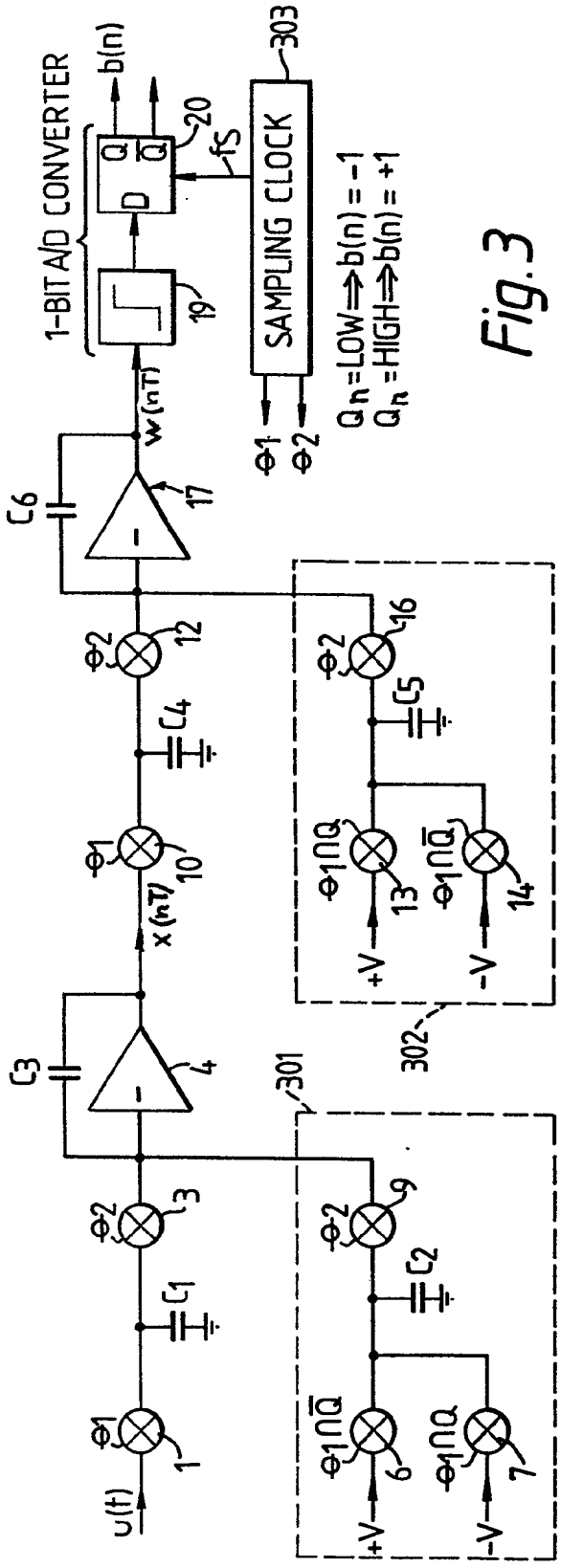

1-BIT A/D CONVERTER
b(n)
20
fs
303
SAMPLING CLOCK
Q
Q̄
D
19
w(nT)
17
C6
Φ1
Φ2
Qn=LOW⇒b(n)=-1
Qn=HIGH⇒b(n)=+1
Φ2
12
16
C4
C5
Φ1
10
Φ1∩Q
Φ1∩Q̄
13
14
+V
-V
x(nT)
C3
4
301
302
Φ2
3
9
C1
C2
Φ1
Φ1∩Q̄
Φ1∩Q
1
6
7
+V
-V
u(t)

Fig. 3

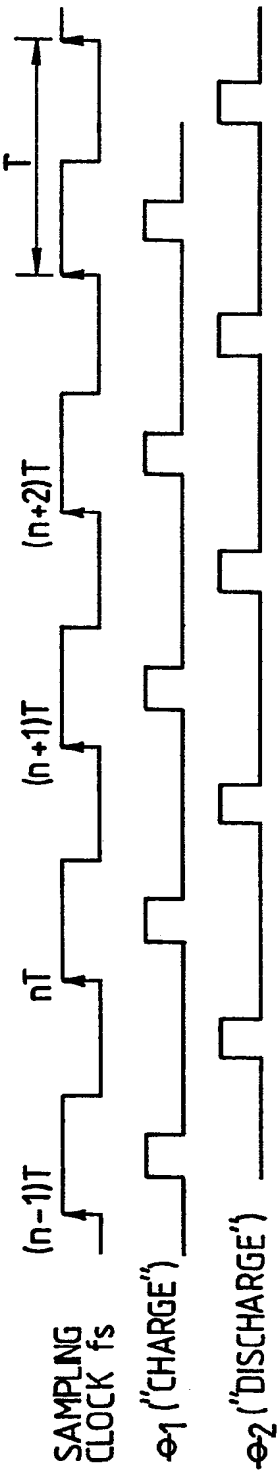
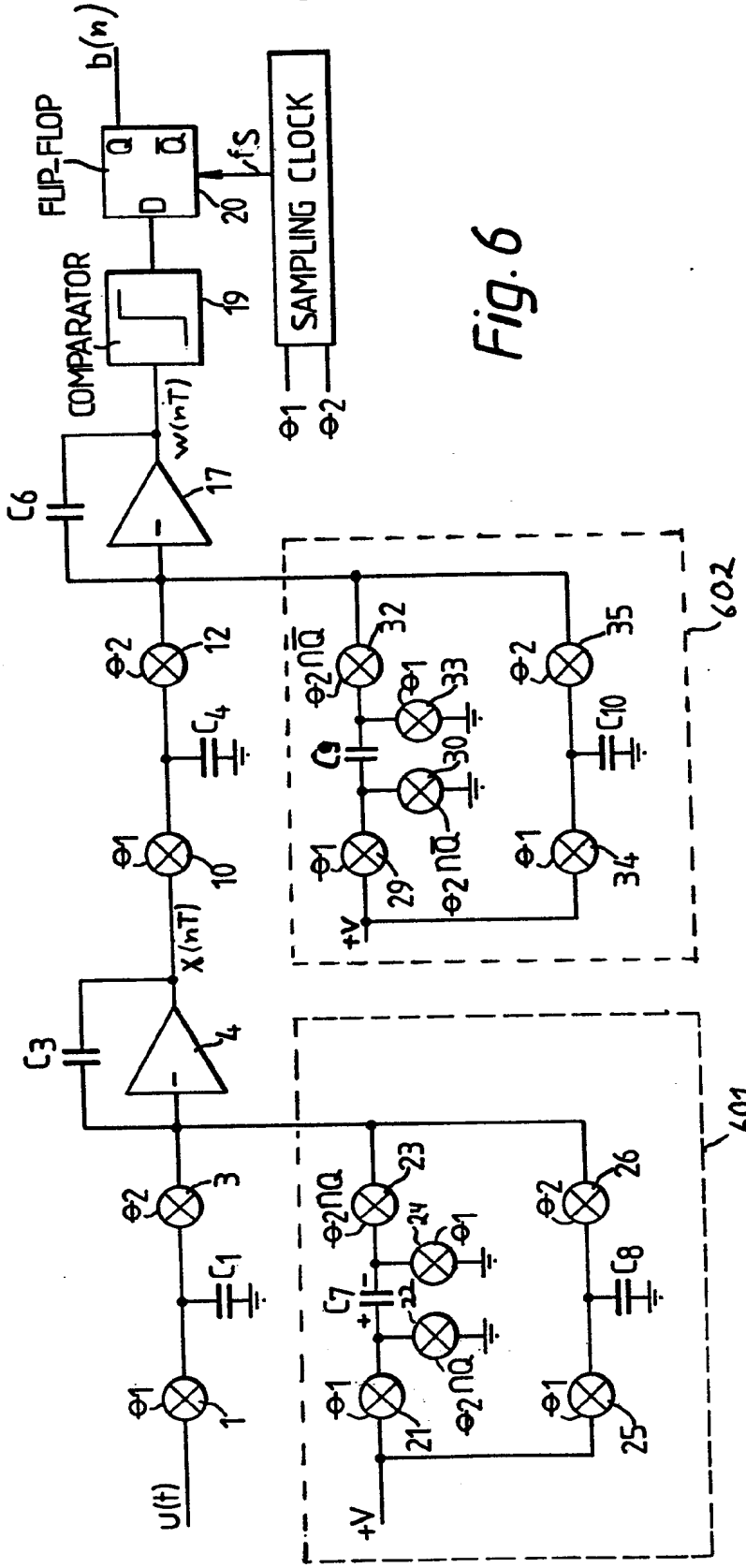

T
(n+2)T
(n+1)T
nT
(n-1)T
SAMPLING CLOCK fs
Φ1 ("CHARGE")
Φ2 ("DISCHARGE")

Fig. 4


b(n)
FLIP-FLOP
Q
Q
D
20
fS
SAMPLING CLOCK
COMPARATOR
19
w(nT)
17
C6
Φ1
Φ2
12
C4
10
x(nT)
C3
4
3
C1
1
U(f)
+V
602
601
32
33
30
29
35
C10
34
C9
C7
22
21
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C8
25

Fig. 6